Ultra-Wide Tuning Range Silicon MEMS Capacitors on Glass with Tera-Ohm Isolation and Low Parasitics

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Abstract— **Theoretical and experimental results of a design methodology and fabrication technology to realize ultra-wide tuning range, electrostatic, silicon micromachined capacitors are presented. The varactors achieve a maximum tuning range of approximately 4000% and exhibit a linear tuning range of 1000% (C vs. V^2). The devices are also designed and characterized with tera-ohm isolation and sub 30fF capacitive coupling between the driving actuator and tuning element. In addition, parasitic capacitances have been minimized to less than 22fF at the tuning element terminals.**

Index Terms— **tunable circuits and devices, capacitors, microelectromechanical devices, varactor, low-parasitic**

I. Introduction

MICRO-ELECTROMECHANICAL tunable capacitors, or varactors, have received a great deal of attention, primarily as components for radio-frequency and microwave applications.[1], [2], [3] Clearly, fixed and tunable capacitors are also critical elements for lower frequency circuits as well. However, the tuning range and capacitances achieved by micromachined devices are too low for many applications. On the other hand, the potential integration of micro-electromechanical systems (MEMS) and integrated circuits as well as the ability of MEMS technologies to achieve extremely low parasitics are highly desirable in many ultra-sensitive, high resolution applications. One such application area is the measurement of minute charge quantities, such as in a sensitive electrometer. Recently an electrometer employing a MEMS capacitor, based on the modulation techniques utilized by vibrating reed electrometers, has been demonstrated. The MEMS based electrometer is capable of measuring 4.5aC (or 28 electrons) at room temperature and pressure [4]; in comparison the state-of-the-art Keithley 6517 exhibits a charge resolution of approximately 10fC (or 63,000 electrons).

Limitations of current micro-electricalmechanical (MEM) tunable capacitors include: low tuning range, high voltage operation, low capacitance per unit area, large parasitics, high mechanical noise sensitivity and coupling of the actuator to the tuning element. Furthermore, MEMS based capacitors are typically shunt devices, one side of the device is tied to ground or a fixed potential. In some applications design trade-offs may allow critical specifications to be met, while allowing compromises in other areas. However, for other applications such compromises are not possible, and an enabling technology is required. By utilizing a silicon on glass fabrication process, decoupling the drive and tuning components as well as employing both area overlap or gap tuning and fringing field disengagement these challenges can effectively be addressed.

The technology developed in this work will allow further enhancement of the previously mention MEMS electrometer design, as well as the development of circuit topologies which can not be achieved employing a shunt capacitor.

II. Device Design and Fabrication

The devices employed in this study are single crystal silicon structures on a glass (Pyrex 7740) substrate. Although silicon-on-insulator (SOI) wafers are readily available, and allow excellent DC isolation between adjacent silicon structures to be achieved the thin (typically sub 4μm, nominal $t_{ox}$is 2μm) buried oxide layer results in large parasitic and stray (or coupling) capacitances. Designing and realizing the devices on a glass substrate allows minimization of parasitic and stray capacitances while maintaining large DC isolations.

The term "parasitic capacitance" encompasses a variety of self and mutual capacitances, and is often not clearly defined. Throughout this paper *parasitic capacitance* will be used to describe the mutual capacitance between a given node and ground. *Stray capacitance* or *coupling capacitance* will be utilized to refer to the capacitive coupling between two non-grounded nodes.

The majority of existing tunable MEMS capacitors consist of a proof mass and one or two sets of electrodes forming a capacitor with the proof mass. In the most common configuration, a single electrode and the proof mass, the proof mass is grounded and a tuning voltage is applied to the electrode (Fig. 1(i)). Due to the applied electrostatic force the electrode is displaced and the capacitance of the structure is increased. A disadvantage of this configuration

is that the design of the actuator and the tunable capacitor are directly coupled, in addition the device is a pure shunt capacitor (one terminal is always grounded). In the second configuration two isolated electrode are employed, one to actuate the proof mass and the second to realize the tunable capacitor(Fig. 1(*ii*)). The advantage of this configuration is that the design of the actuator and the tuning capacitor can be partially decoupled and there is a DC isolation between the actuation and signal paths. However, the proof mass is still connected to a common potential.

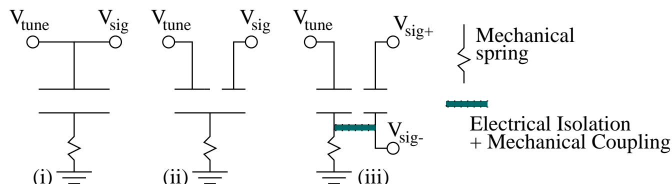

Fig. 1. Simplified representations of different types of MEMS capacitors (*i*) a shunt capacitor with a single terminal for the drive and signal paths (*ii*) a shunt capacitor with seperate terminals for the drive and signal paths and (*iii*) a capacitor with electrically isolated drive and signal paths.

In this work a nitride isolation technology is employed to achieve electrical isolation and mechanical coupling between the drive and tuning components of a MEMS based varactor in order to realize a true two terminal variable capacitor (Fig. 1(*iii*)). Therefore the design of the actuator and the tuning element are decoupled and may be independently optimized.[1] In addition, the tunable capacitor may be employed as a parallel or series element between any two nodes, rather than simply as a shunt component. Isolation technologies have been developed in the past for actuation and current measurement, such as in [5]; however, the parasitics have been too large for high sensitivity electrometers and other applications sensitive to large parasitics. Recently large tuning range capacitors with isolation have concurrently been demonstrated, [6]; in this case the mechanical stability, coupling capacitance and surface resistivity of the isolation material are not sufficient to meet the stringent requirements of this work.

A. Fabrication Process

An overview of the fabrication process developed in this work is presented in Fig. 2; this process is built on previous single crystal silicon on glass work.[7], [8] In this process a heavily doped silicon wafer is etched to define multi-level beams and isolation trenches, which are refilled with a high-conformality low-stress nitride to later serve as electrical isolators and mechanical coupling structures. The silicon wafer is then anodically bonded to a 7740 Pyrex wafer. Following thinning and polishing of the silicon device layer a second high aspect ratio DRIE is performed to define the devices.

[1]It should be noted that an electrostatic force will be generated between the sense path electrodes if a potential is present; therefore the design of the actuation and tuning segments may not truly be considered to be fully decoupled.

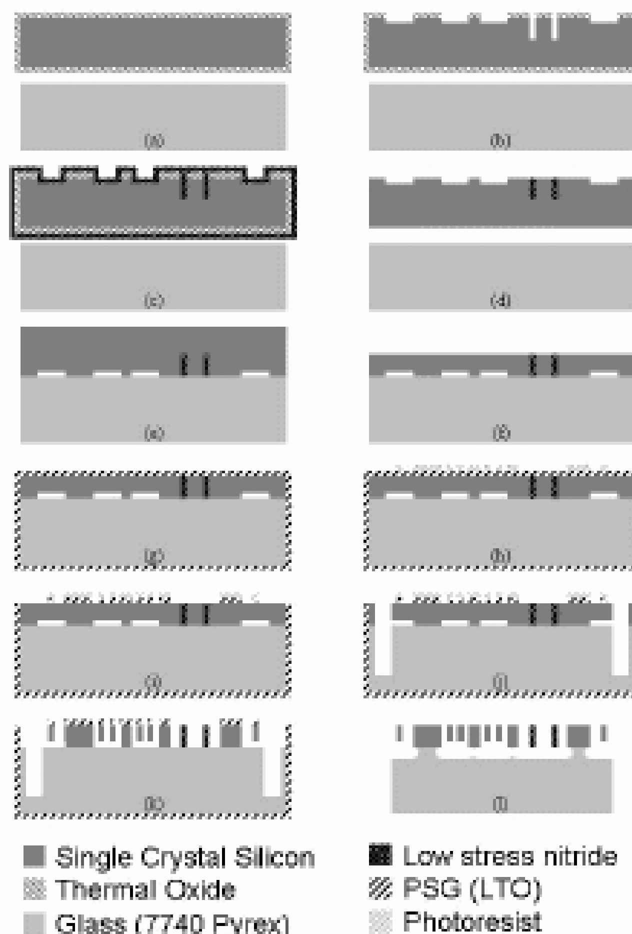

Fig. 2. A schematic diagram outlining the silicon on glass fabrication process with nitride isolation structures, refer to text for the process description.

The fabrication process is initiated with two separate wafers, a high conductivity silicon wafer and a 7740 Pyrex wafer; a 1μm thermal oxide layer isgrown on the silicon wafer to protect the bonding surface and also serve as a hardmask (Fig. 2a). Utilizing two self aligned masks multilevel trenches may be etched in the silicon wafer (Fig. 2b) in two deep reactive ion etch (DRIE) steps. High-aspect ratio (>50:1) deep trenches are etched to define isolation structures, which will later be refilled with nitride. The deep etch also creates alignment marks for subsequent processing. The second, more shallow, set of etches is optional and may be employed to provide release trenches or multilevel silicon beams. In the next step of the process, (Fig. 2c), a highly conformal, low-stress (<80MPa) CVD nitride is deposited for isolation trench refill. The planar nitride is then removed from the backside and frontside of the silicon wafer, and the protective oxide layer is stripped (Fig. 2d). Next the silicon and Pyrex wafers are anodically bonded, with the previously processed side of the Si wafer at the bond interface (Fig. 2e). As depicted in (Fig. 2f) the silicon wafer is then thinned to the desired thickness and a chemical mechanical polishing (CMP) step is performed to provide a high quality, polished device layer

surface; in this step the deep isolation trenches and alignment marks are exposed. The bonded wafer pair is then conformally coated with a 2μm layer of low temperature oxide (LTO), (Fig. 2g). A photolithography step carried out to define the device regions (Fig. 2h) and the LTO hardmask is patterned (Fig. 2i). The glass wafer is then partially diced (Fig. 2j). In the next step the most critical high aspect ratio (>75:1) DRIE is completed, defining the device structures (Fig. 2k). In this final device etch all non-device silicon is removed in order to minimize parasitic and stray capacitances. Finally the die are individually cleaned and released in a hydrofluoric acid etch (Fig. 2l). This etch releases the full thickness structures and also serves to decrease undesired capacitances by increasing the gap between the conductive Si and the insulator. Furthermore, the cleaning step and the release etch insure the removal of any metals or organics which would result in a shunt resistance.

A schematic diagram showing the key device components is presented in Fig. 3.

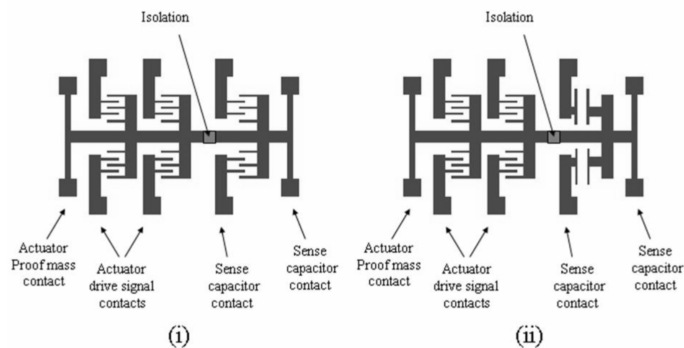

Fig. 3. A simplified schematic diagram showing two types of devices: (*i*) a comb-driven actuator with a comb-finger tunable capacitor and (*ii*) a comb-driven actuator with a parallel plate tunable capacitor. Also shown are the contact areas and isolation structure.

B. Actuator Design

As the actuator and the tuning element are decoupled the trade-offs associated with each may be considered somewhat independently. For example, to achieve a lower driving voltage the size (capacitance) of the driving actuator may be increased, with proper design the coupling of the drive signal to the sense signal path can be minimized and the primary concerns are the area-footprint and resonant frequency of the device.

Comb-drive actuators are chosen for the drive component of the device as they can be designed to have long actuation ranges and require minimal power. Furthermore, comb-drive actuators are able to deliver a linear (with the square of applied voltage) force over a wide range of positions. The well know expression for the force developed by a comb-finger based actuator in air is:

$$F_{cd} = N_B N_f \epsilon_0 \frac{h}{g} V^2 \tag{1}$$

where N_B is the number of comb-finger banks, N_f is the number of fingers per bank, ϵ_0 is the permittivity of free space, h is the height or thickness of the comb-fingers, g is the gap distance between fingers and V is the applied voltage. Clearly in addition to simply increasing the number of fingers it is desirable to realize thick structures with narrow gaps, hence one of the objectives driving the development of the very high aspect ratio fabrication process.

C. Tuning Capacitor Design

As the tuning element is not required to generate a force, and in fact it is desirable that it does not, extremely small capacitances may be realized. In applications such as a modulated input capacitance for an electrometer the modulation depth of the capacitance should be maximized while both the parasitics and minimum value of the tunable capacitor should be minimized [4].

Two tuning capacitor elements are employed. The first is a parallel plate structure, normally parallel plate capacitors are limited to 1.5:1 tuning ratios due to instability, however, as long as the position of the proof mass is controlled by the actuator section this instability can be overcome and large tuning ranges achieved. The first order expression for the capacitance of the parallel plate structure is given by:

$$C_{pp} = \epsilon_0 \frac{wl}{x} \tag{2}$$

where w is the width of the plates, l is the length and x is the gap distance. The force applied due to a voltage V_{sig} across the structure is:

$$F_{pp} = \frac{1}{2} \epsilon_0 \frac{wl}{x^2} V_{sig}^2 \tag{3}$$

The second tuning element is a comb-finger based capacitor, as long as the fingers are engaged by approximately $3\times$ the gap distance the capacitance, ignoring second order effects, is:

$$C_{cf} = 2 N_B N_f \epsilon_0 \frac{h x_{ov}}{g} \tag{4}$$

where x_{ov} is the overlap distance. The force exerted by a voltage V_{sig} will be:

$$F_{cd} = N_B N_f \epsilon_0 \frac{h}{g} V_{sig}^2 \tag{5}$$

If the overlap distance (x_{ov}) is allowed to approach zero, and eventually fully disengage, the fringing field components of the electrical fields will begin to dominate the capacitance. If the fingers are disengaged by several gap distances the capacitance begins to resemble that of two plate structures. Utilizing this fact very large modulation depths may be achieved; a large capacitance is realized when the fingers are maximally engaged and a very small capacitance is achieved by fully disengaging and separating the fingers. It should be noted this capacitance change is not linear, the while the fingers are engaged a linear C vs. V^2 relationship will be observed (dC/dx is constant); however, during disengagement the magnitude of dC/dx will

increase significantly. The shape of the C vs. V curve is highly dependent on the geometry of the comb-finger tips.

More complete analytical models of the variable capacitance, parasitics and strays are taken into account when designing and modeling the structures. In addition, finite element analysis utilizing ANSYS and HFSS are used to facilitate the design.

D. Stability, Noise, Parasitics and Strays

Amplitude and phase noise as well as the effect of external accelerations must be carefully considered during the design process. It is also necessary to consider the effect of process variations on device dimensions and therefore the electrical and mechanical properties of the device. Furthermore, although typically small the effect of absorption and desorption as well as Brownian motion are potential concerns. A more complete discussion of noise sources and analysis techniques is provided in [9].

Parasitic capacitances are minimized by the fabrication of the devices on a glass substrate, further minimization is achieved by removing excess blocks of grounded silicon and maximizing the gap between the silicon devices and the Pyrex substrate when the devices are released. The stray, or coupling capacitances, are minimized by removing excess silicon surrounding the devices and also by physically separating the drive and signal path components.

III. Results

The devices presented in this work are realized on a 500μm thick Pyrex handle wafer with a 100μm thick silicon device layer. A photograph of several fabricated devices next to a dime is provided in Fig. 4.

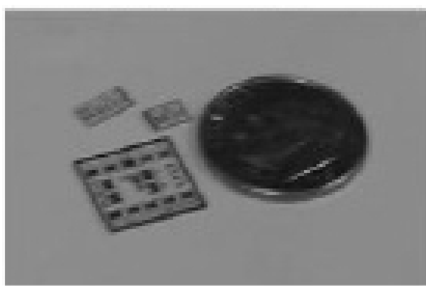

Fig. 4. A photograph of fabricated device die next to a dime, the large die is 10mm×10mm and the thickness of the silicon device layer is 100μm.

SEMs of two fabricated devices are presented in Fig. 5a and 5b. The device in Fig. 5a has a parallel plate tuning element driven by a comb-finger actuator. In Fig. 5b the same actuator is employed to drive a comb-finger based capacitor.

The nominal suspension springs (Fig. 5c) widths are between 1.5μm and 3.5μm. The actuation comb-fingers (Fig. 5d) are 30μm long with a 3μm width and spacing. The comb-fingers of the tuning element (Fig. 5b) are 2μm wide with a 1.5μm gap distance. The nitride isolation beams (Fig. 5e) are 2μm wide, 15-20μm long and 100μm thick.

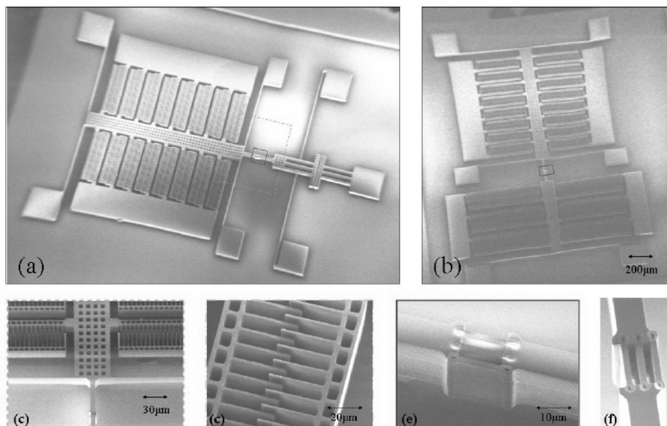

Fig. 5. SEMs of fabricated and released 100μm thick devices: *(a)* a parallel plate tuning element driven by an interdigitated comb-drive actuator, *(b)* a comb-drive actuator and tuning component, *(c)* an image showing the comb-drive actuators, suspension springs and electrical isolation structure, *(d)* a close-up of the comb-fingers, *(e)* the nitride isolation beams, *(f)* even in the case of misalignment nitride beam stress is not an issue.

A. Measurement and Device Characterization

Electrical and mechanical characterization of the fabricated devices is performed employing unpackaged as well as custom packaged die. Displacement measurements are achieved optically (vertical camera and lateral laser Doppler vibrometer) as well as via a capacitance measurement circuit. The capacitance of the tuning element as a function of a static applied tuning voltage is measured utilizing a LCR meter as well as a custom capacitance measurement circuit. The capacitance under AC drive conditions is measured using the custom capacitance measurement circuit. The capacitance measurements are performed at frequencies between 100kHz and 1MHz with a measurement signal amplitude of 50mV.

Several sets of devices are realized on each die with varying designs; the largest tuning range devices have an initial capacitance of 2.05pF, a minimum linear (vs. V^2) capacitance of 195fF and an absolute minimum capacitance of 48fF. A plot of capacitance vs. tuning voltage is provided in Fig. 6.

This device exhibits the lowest mechanical resonant frequency of the fabricated devices, 1.5kHz with a quality-factor (Q) of 40. A plot of normalized displacement vs. frequency is shown in Fig. 7.

The DC isolation across the nitride isolation structure, and through the glass, between the actuation and tuning capacitor contacts connected to the proof mass is measured using a probe with femto-amp resolution. The minimum measured isolation was 5TΩ, with a typical value $\geq$20TΩ. A plot of current vs. applied voltage is given in Fig. 8, the isolation is approximately 26TΩ.

The parasitic capacitance at the tuning element terminals is measured to be less than 22fF. The coupling capacitance between the drive electrodes and either terminal of the tunable capacitor is at most 30fF.

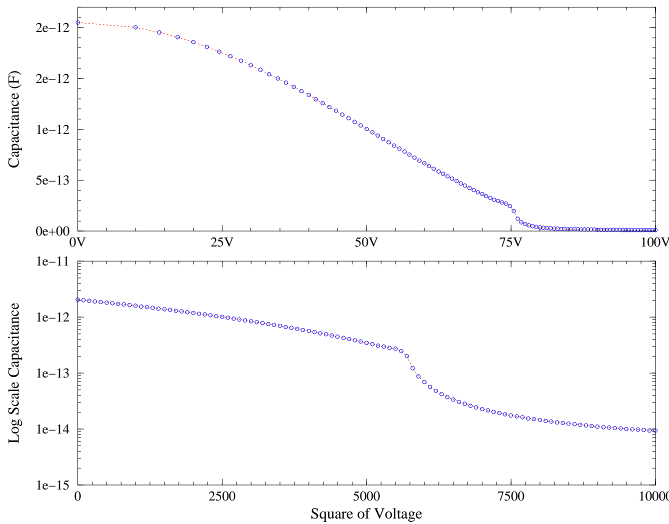

Fig. 6. Capacitance vs. voltage, the tuning ratio is 42.7:1 (C_{max}=2.05pF, C_{knee}=195fF, C_{min}=48fF)

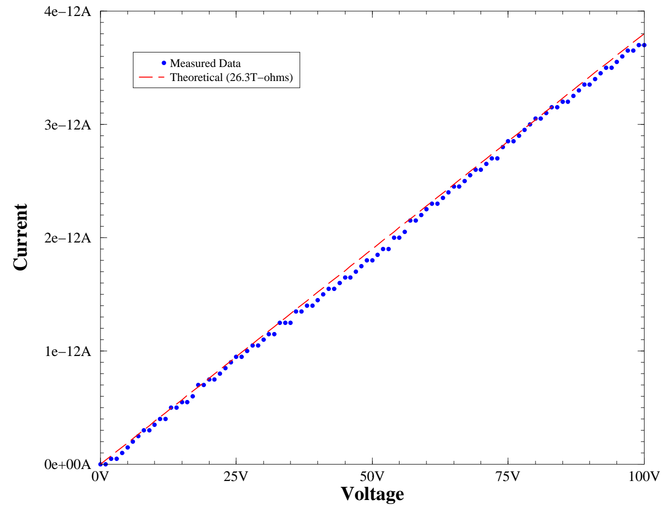

Fig. 8. Measured isolation from the drive proof-mass to the sense proof mass, approximately 26TΩ.

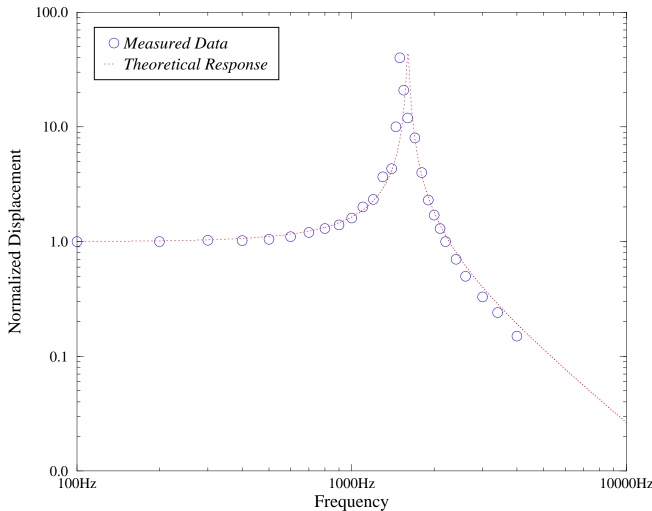

Fig. 7. The mechanical frequency response of the reported device (f_r=1.5kHz, Q≈40)

IV. Conclusion

A fabrication technology allowing the realization of high aspect ratio single crystal silicon structures on glass with electrical isolation structures has been demonstrated. Devices fabricated in this technology have exhibited modulation depths as high as 42.7:1 with extremely low parasitic capacitances and excellent DC isolation. In addition, the isolation allows two terminal, floating capacitors to be realized, permitting the devices to be employed in a wide range of circuit topologies.

Although this technology has been developed for low frequency applications requiring large modulation depth, low minimum capacitance, excellent isolation and ultra-low parasitics, such as electrometers, it is readily adaptable to other applications, including RF and microwave systems.

Future work will continue investigation of these devices for use in electrometers and electric field meters and will also focus on adapting the fabrication technology for RF and microwave applications. Additionally, efforts will continue to be taken to minimize the effects of process variation.

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